P-TDC

Features

- High resolution mode, 64 channels with 100 ps LSB resolution
- Very high resolution mode,16 channels with 25 ps LSB resolution
- Programmable acquisition modes (triggered or continuous)
- Hit inputs accept LVDS or LVTTL logic standards
- Maximum random data rate of 2 MHz per channel
- Global sustained event rate of approximately 5 MHz, with up to 40 MHz burst rate
- USB 2.0 readout
- DLL available supporting up to 8 connected modules
- Clock inputs and outputs for timing synchronisation

Applications

- Fluorescence Lifetime Imaging (FLIM)
- Förster Resonant Energy Transfer (FRET)
- High Energy Physics
- Light Detection and Ranging (LIDAR)
- Nuclear Physics
- Particle Physics
- Quantum Cryptography Research
- Single Molecule Detection
- Scanning Microarrays
- Sub-atomic Physics
- Time resolved medical imaging & diagnosis
- Time-of-flight Positron Emission Tomography (TOF-PET)

General Description

The P-TDC is a high time resolution time to digital convertor (TDC), which provides an integrated picosecond resolution timing solution for photon detectors using suitable front end pre-amplifier and discriminator electronics. The P-TDC utilises the HPTDC ASIC developed at CERN for ALICE time of flight systems. The P-TDC incorporates an onboard FPGA for application specific control/data processing and USB readout in a footprint suitable for bench-top experiments, and applications with tight space requirements. Up to 8 P-TDCs can be used on one computer providing 512 100 ps channels or 128 25 ps channels.

Operation of the module is configurable with two time resolution modes (100 ps and 25 ps time binning), triggered or continuous readout and LVDS or LVTTL inputs. When used in conjunction with Photek's single photon detectors, which offer best in class timing performance, the system forms a high performance platform for a diverse range of applications in Physics, Biology, Life Sciences, Medical Imaging and Astronomy.

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Technical Specifications

- 64 Channel and 16 channel options
- 50 Ω LVTTL or LVDS logic input options
- Combined measurement of leading and trailing edge times
- Trigger matching mode, for selecting events within a configurable time window (25 ns to 100 µs). Timestamps configurable to be relative to the trigger edge or global clock.
- Continuous readout mode to run without a trigger.
- Clock inputs/outputs for synchronisation with external equipment
  - Internal free running 40 MHz clock
  - 40 MHz 50 Ω LVTTL clock input
- 5 MHz maximum global rate
- Trigger buffer size 16
- 4096 event buffer size
- 75 ns dead time

High Resolution Mode

- Bin size of 97.656 ps, this is calculated from $\frac{\text{Clock Period}}{256} = \frac{25\text{ ns}}{256} = 97.656\text{ ps}$
- Dynamic range of 19 bits (52.4 µs)
- Per channel maximum rate
  - 2 MHz for all 64 channels
  - 4 MHz when every second channel is used (i.e. channels 0, 2, 4, 6... are used giving a total of 32 channels)

Very High Resolution Mode

- Bin size of 24.414 ps, this is calculated from $\frac{\text{Clock Period}}{1024} = \frac{25\text{ ns}}{1024} = 24.414\text{ ps}$
- Dynamic range of 21 bits (52.4 µs)
- Per channel maximum rate of
  - 4 MHz for all 16 channels
  - 8 MHz when every second very high resolution channel is used (i.e. channels 0, 8, 16, 24... are used giving a total of 8 channels)

Timing Performance

- Random timing jitter typically <20 ps (see Figure 1)
- Propagation delay between two channels ±1 ns, 100 ps variation per 10°C
- Pre-calibrated Integrated non-linearity (INL) correction (see Figure 2)
  - <0.5 LSB RMS, for entire dynamic range of 52 µs.
  - INL correction is also user configurable for best performance in your environment

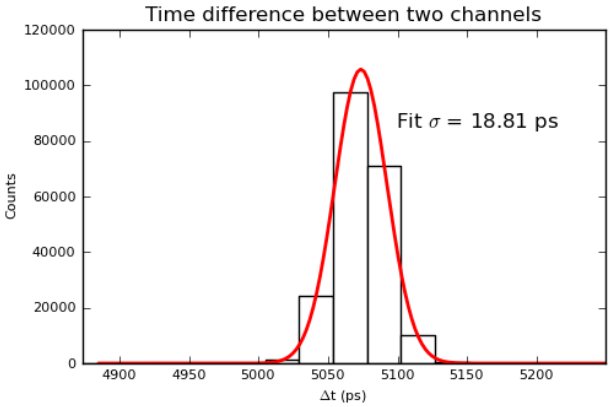

Figure 1 - A histogram showing the distribution of the time difference between two synchronised pulses fed in to two channels (24.41 ps time bins). The fitted Gaussian gives a random timing jitter of 18.81 ps RMS.

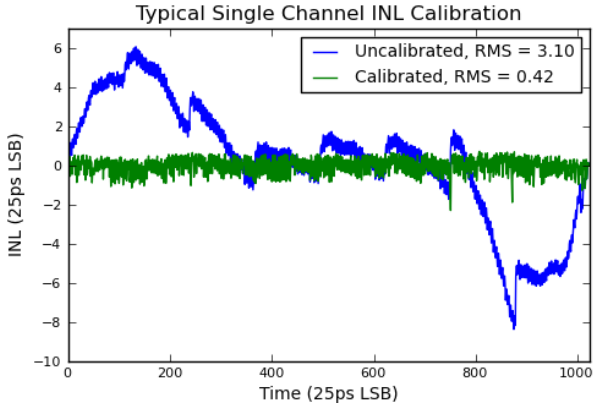

Figure 2 – The uncalibrated plot shows the typical INL of a single channel of a HPTDC ASIC. The calibrated plot shows a typical INL for the P-TDC module with the default INL correction enabled.

Electrical & Mechanical

Electrical: 6 – 12 VDC @ 2 A

Operating Temperature: 0°C to 40°C

Dimensions 165 x 60 x105 mm (L x H x W)

Photek Ltd reserves the right to update and improve this specification without prior notice

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